AMENDMENTS TO THE CLAIMS

The following listing of claims shall replace all prior versions, and listings, of Claims in the present application:

LISTING OF CLAIMS:

1. (Currently Amended) A double-high memory system compatible with termination schemes for single-high memory systems comprising:

an interface for input and output of data;

a plurality of memory units configured in two rows; and

a transmission line coupling said plurality of memory units to said interface, wherein a double-high memory module is provided in a non-stacked arrangement, and wherein said plurality of memory units is coupled together in a daisy chain configuration.

2. (Cancelled)

3. (Cancelled)

4. (Original) The double-high memory module of Claim 1, wherein an impedance is situated between said connector and said two memory units.

5. (Cancelled)

6. (Cancelled)

7. (Original) The double-high memory module of Claim 4, wherein said impedance is a resistor.

8. (Original) The double-high memory module of Claim 4, wherein said impedance is a 22 ohm resistor.

9. (Original) The double-high memory system of Claim 1, wherein said memory modules are dual inline memory modules.

10. (Original) The double-high memory module of Claim 1, wherein said memory units are DDR SDRAM.

11. (Currently Amended) The double-high memory module of Claim [[2]] 1, wherein said third transmission line is one inch in length.

12. (Original) A system comprising:

a bus controller;

a plurality of memory module connectors coupled to said bus controller;

a single-high memory module coupled to a first of said connectors;

a double-high memory module coupled to a second of said connectors;

said double-high memory module comprising:

an interface for input and output of data;

a plurality of memory units configured in two rows; and

a transmission line coupling said plurality of memory units to said interface, wherein a double-high memory module is provided in a non-stacked arrangement.

13. (Original) The double-high memory module of Claim 12, further comprising a second transmission line connected to the first of two memory units that are coupled together via a third transmission line in a daisy chain configuration.

14. (Original) The double-high memory module of Claim 12, further comprising two separate equal length transmission lines, wherein each of said equal length transmission lines connects to one of two memory units.

15. (Original) The double-high memory module of Claim 12, wherein an impedance is situated between said connector and said two memory units.

16. (Original) The double-high memory module of Claim 14, wherein said two separate transmission lines are symmetrically configured and signal transmission is balanced on each of said transmission lines.

17. (Original) The double-high memory module of Claim 14, wherein each of two substantially equal length transmission lines connects to one of two memory units.

18. (Original) The double-high memory module of Claim 15, wherein said impedance is a resistor.

19. (Original) The double-high memory module of Claim 15, wherein said impedance is a 22 ohm resistor.

20. (Original) The double-high memory module of Claim 12, wherein said memory module is a dual inline memory module.

21. (Original) The double-high memory module of Claim 12, wherein said memory units are DDR SDRAM.

22. (Original) The double-high memory module of Claim 13, wherein said transmission line is one inch in length.

23. (Currently Amended) A method for operating a double-high memory system compatible with termination schemes for single-high memory systems comprising:

receiving data into an interface for input and output of data; and

storing and retrieving data from a plurality of memory units configured in two rows, wherein

a transmission line couples said plurality of memory units to said interface, [[and]] wherein said double-high memory module is provided in a non-stacked arrangement, and wherein said plurality of memory units is coupled together in a daisy chain configuration

24. (Cancelled)

25. (Cancelled)

26. (Original) The method Claim 23, wherein an impedance is situated between said interface and said two memory units.

27. (Cancelled)

28. (Cancelled)

29. (Original) The method of Claim 26, wherein said impedance is a resistor.

30. (Original) The method of Claim 26, wherein said impedance is a 22 ohm resistor.

31. (Original) The method of Claim 23, wherein said memory module is a dual inline memory module.

32. (Original) The method of Claim 23, wherein said memory units are DDR SDRAM.

33. (Currently Amended) The method of Claim [[24]] 23, wherein said transmission line is one inch in length.